REMARKS

Fig. 1 is amended.

Claims 1-4 and 6-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Uemura, U.S. Patent Application Publication 2003/0222270. Claims 5 and 10-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uemura in view of Yagi et al., U.S. Patent Application Publication 2002/0070449 (U.S. Patent 6,642,618) and Horiuchi et al., U.S. Patent Application Publication 2003/0094622. Applicants respectfully traverse the rejections.

Claim 1 is amended to recite "a submount comprising . . . a semiconductor region; and an insulating region." Applicants have found no teaching in Uemura, Yagi et al., or Horiuchi et al. of a submount having both a semiconductor region and an insulating region. Fig. 6 of Uemura states only that structure 61, cited by the Examiner as being claim 1's submount, is a "board," see paragraph 75. Yagi et al., teaches a substrate 101 that "is typically a wiring board of epoxy resin or other plastic, but is not limited thereto. The substrate has formed thereon a dielectric layer 101a of plastic or the like, over the dielectric layer 101a, a suitable pattern of conducting paths 101b . . . ." See column 4, lines 37-42 of U.S. Patent 6,642,618. Yagi et al. further teach a submount 108 that "may be fabricated from materials such as silicon, ceramic, metal, etc. In the present example, submount 108 is provided with conducting portions (namely electrode portions 109) for electrical connection with the metal bumps 103 and with conductive paths 110 leading from the electrode portions 109." See column 6, lines 32-38 of U.S. Patent 6,642,618. Horiuchi et al. teach "a substrate 2, made of liquid crystal polymer and having a semispherical recess 4 . . . ." See paragraph 14. Accordingly, since none of the references relied upon by the Examiner, either alone or in combination, teach a submount having both a semiconductor region and an insulating region, claim 1 is allowed over Uemura, Yagi et al., and Horiuchi et al.

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Claims 2-12 and 14-26 depend from claim 1 and are therefore allowable for at least the same reason as claim 1. In addition, regarding claim 5, Applicants can find no teaching in Uemura, Yagi et al., or Horiuchi et al. of "first and second conductive layers [that] are highly doped semiconductor layers." Claim 5 is thus allowable for this additional reason. Regarding claim 8, Applicants can find no teaching in Uemura, Yagi et al., or Horiuchi et al. of "first and second conductive layers [that] each at least partially surround a region of semiconductor material within the submount." Claim 8 is thus allowable for this additional reason. Regarding claims 17-20, 25, and 26, Applicants can find no teaching in Uemura, Yagi et al., or Horiuchi et al. of the areas, current density, current, and electrical power consumption recited in these claims. Claims 17-20, 25, and 26 are thus allowable for this additional reason.

In view of the above arguments, Applicants respectfully request allowance of claims 1-12 and 14-26. Should the Examiner have any questions, the Examiner is invited to call the undersigned at (408) 382-0480.

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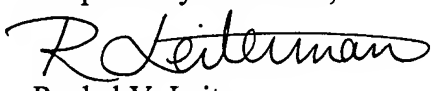

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IN THE DRAWINGS

The attached sheet of drawings includes changes to Fig. 1. This sheet, which includes only Fig. 1, replaces the original sheet including Fig. 1.

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